REMARKS/ARGUMENTS

New substitute formal drawings are submitted herewith. Figure 1 has been labeled PRIOR ART.

The undersigned wishes to thank the examiner for his careful examination, and accordingly there are changes correcting the errors noted regarding 35 USC 112. Claim 6 has been made an independent claim.

Reconsideration on the claims is requested. The claim changes suggested by the examiner make this much more clear. However, the reference cited Watai Patent 57545373 does not relate to or show an orthogonality checker, so no anticipation by the reference is shown.

FIG 1 of the application shows prior art where all combinations of two inputs are ANDed and output is ORed in one level of logic (several ANDs followed by one OR).

The Watai patent 5745373 does not address the nature of orthogonality checkers at all, and orthogonality checker is a claim limitation for all claims. They focus only on fanout and loading to minimize number of stages in a general logic structure. Their FIG 3 and 4 looks similar to elements of the applicants illustrated FIG1, logically, but Figure 1 logic is not what the applicants are claiming. They obviously focus on buffering to help optimize WITHIN a function. Their logic is not an orthogonality checker anyway. They have AB, AC, AD, but are missing BC, BD, and CD.

Watai patent 5745373 uses a technique to analyze loading, assigning cells, counting stages, and iterating through that to find a combination of cells and gates.

The applicants take a large orthogonality checker and optimally break it down into an efficient hierarchy of smaller, enhanced, orthogonality checker building blocks by the step of using a library of logical gates to implement a minimized ~~the~~ circuit and the area for each logical gate in the library. Watai's patent 5745373 dosen't teach this at all.

The applicants' claims are specific to ORTH checkers. The Watai reference may seem more general, but theirs does not teach what is taught and claimed by the applicants.

- Watai makes no mention of multiple-levels of building blocks we refer to as ORTH opthogolality checker.
- The applicants' levels are AND/OR along with a parallel OR. Watai dosen't mention this at all, a prerequisite to using our invention. Watai's Fig. 3 and Fig. 4 don't show show a circuit.

- Watai only shows one level of logic in a 'cell', e.g. AND. The ortoogolality checker ORTH is different than that.
- Watai does not show how to minimize gates or area. The Watai focus is only on timing and stages.
- Watai's timing is based strictly on capacitance loading and fanout and longest stage. Watai doesn't mention total area or total gates or look-up tables for how to optimize orthogonality checkers.

The applicants' Figure 4 shows one example of how a larger ORTH can be broken down into smaller ORTH functions with the inclusion of some extra ORs.
The applicants' Figure 3a shows how a 6-way orth can be made by cascading two 3-way ORTHs through a 2-way ORTH. This can save area and gates.

These differences are within the scope of the claims sought by the applicants.

This application is believed to be in condition for allowance and notice thereof is requested.

Respectfully Submitted,
For the Inventor(s):

By _____ Date: Ocotober 6 , 2006_____
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SUBSTITUTE DRAWINGS ARE INCLUDED IN THE APPENDIX WHICH FOLLOWS.